



Power Good ASIC SF401104

DESCRIPTION

The main application of the Power Good ASIC is to monitor the outputs of switched mode power supplies during start up and running, and to respond in the event of an undervoltage or overvoltage condition on one or more of the monitored inputs.

Timing controlled within the ASIC avoids false signalling due to transients.

The configuration of the ASIC allows up to 5 supplies to be monitored, 3 positive and 2 negative. The following can be monitored without the need for external components: +12V, +5V, +2.175V, -12V and -5V.

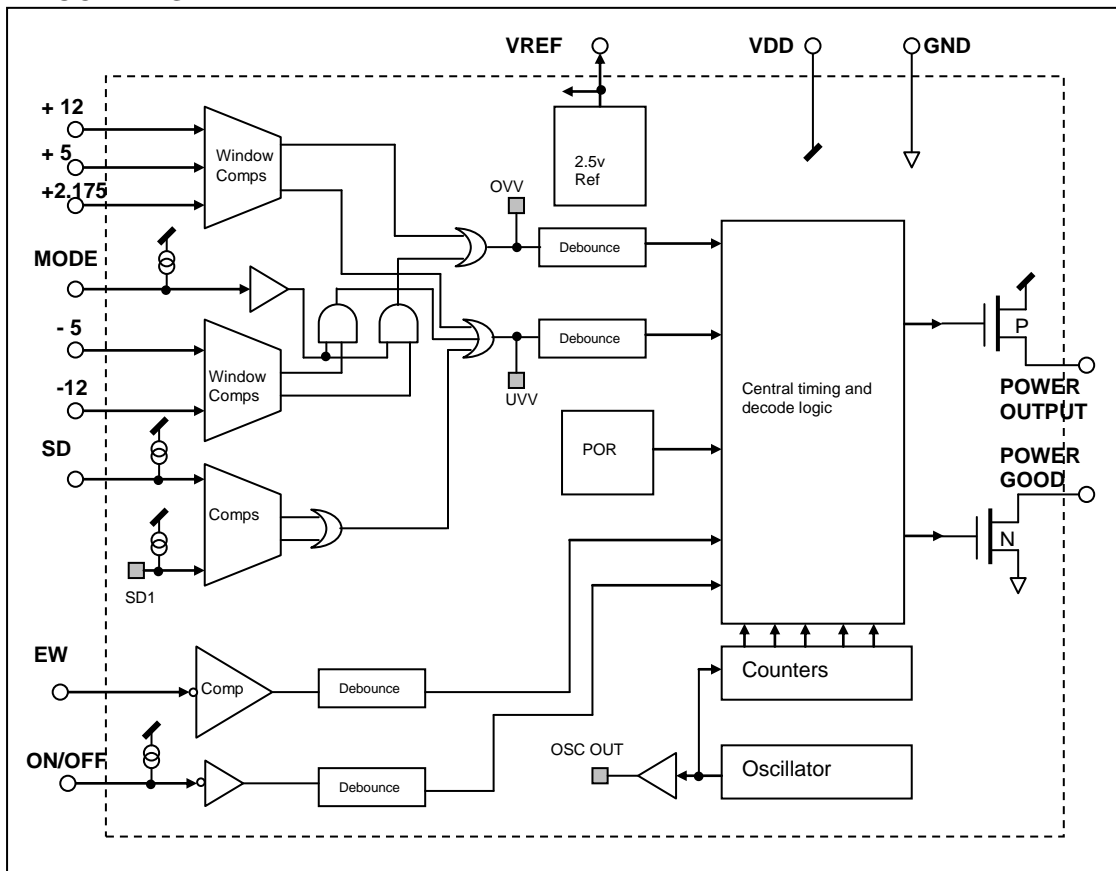
FEATURES

- 5 supplies monitored
- Positive and negative supply monitoring
- Response to shutdown signalling
- Logical fault differentiation
- Input power loss sensing
- Time outs to prevent false signalling
- Digital debounce on inputs
- Accurate, band gap voltage reference

APPLICATIONS

- PC power supply monitor
- Un-interruptable power supplies

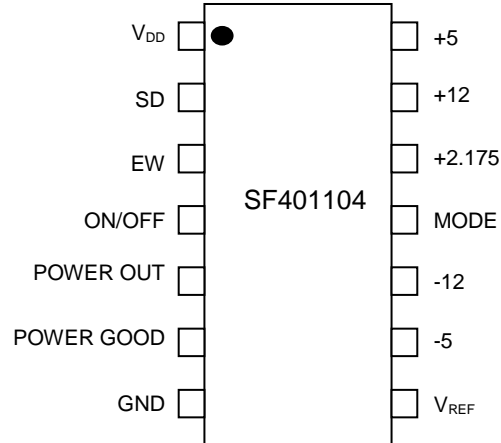
BLOCK DIAGRAM



PIN CONFIGURATION



These devices have been designed to withstand up to 1kV of electrostatic discharge between pin pairs. As such, precautions must be taken to ensure that the device is not damaged during handling and transportation.



PIN DESCRIPTION for 14 PDIP

NAME	PIN	TYPE	FUNCTION
V _{DD}	1	Supply	Supply voltage
SD	2	Analogue Input	Shut down
EW	3	Digital Input	Early warning
ON/OFF	4	Digital Input	On/off control direct from PSU switch.
POWER OUT	5	Digital Output	Power output status. (open drain output)
POWER GOOD	6	Digital Output	Power good status (open drain output)
GND	7	Supply	Ground
V _{REF}	8	Analogue Output	+ 2.5V reference voltage
-5	9	Analogue Input	-5V monitor
-12	10	Analogue Input	-12V monitor
MODE	11	Digital Input	3 or 5 supply monitor selector.
2.175	12	Analogue Input	+ 2.175V monitor
+12	13	Analogue Input	+12V monitor
+5	14	Analogue Input	+5V monitor

Note. There are extra pads available on the ASIC for bonding out. These are SD1, OSC OUT, OVV and UVV. Contact the factory if your application needs an alternative package or pinout.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply voltage V _{DD}	8.14	V
Operating Temperature, T _O	0 to 85	°C
Storage Temperature, T _S	-40 - +105	°C

ELECTRICAL SPECIFICATION

Test conditions $V_{DD} = 4.0V$ to $8.0V$, MODE pin = Hi unless otherwise stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{REF} , reference output voltage.	0 to $85^{\circ}C$	2.47 -1.5	2.5 -	2.53 +1.5	V %
I_{REF} , current loading on V_{REF}		-100		+100	μA
CLK ⁽¹⁾	$V_{DD} = 5.0V$	30	32	34	kHz
I_{DD}	$V_{DD} = 8.0V$		2	3	mA
Threshold voltage, EW, input	Active when < value	2.45 -1.7	2.5 -	2.54 +1.7	V %
Threshold voltage, SD and optional SD1 inputs	Active when > value	2.37 -5	2.5 -	2.62 +5	V %
ZIN_{+12} , input impedance	Referenced to GND		10		Kohm
ZIN_{+5} , input impedance	Referenced to GND		5		Kohm
$ZIN_{+2.175}$, input impedance	Referenced to GND		1000		Kohm
ZIN_{-5} , input impedance	Referenced to V_{REF}		25		Kohm
ZIN_{-12} , input impedance	Referenced to V_{REF}		50		Kohm
ZIN_{EW} , input impedance	Referenced to GND		1000		Kohm
$I_{in_{ON/OFF}}$, input current	Pin to GND	-20	-	-40	μA
$I_{in_{SD}}$, input current	Pin to GND	-20	-	-40	μA
$I_{in_{MODE}}$, input current	Pin to GND	-20	-	-40	μA
$I_{out_{POWER OUTPUT}}$, active output current	Drain voltage = $V_{DD} - 1V$	-10	-		mA
$I_{out_{POWER OUTPUT}}$, inactive leakage current	Drain voltage = $V_{DD} - GND$		+/- 1		μA
$I_{out_{POWER GOOD}}$, active output current	Drain voltage = 0.38V	10			mA
$I_{out_{POWER GOOD}}$, inactive leakage current	Drain voltage = 13V		+/- 1		μA
$V_{ih_{MODE}}$, input logic HI level		TBD			V
$V_{il_{MODE}}$, input logic LO level		TBD			V
$V_{ih_{ON/OFF}}$, input logic HI level		TBD			V
$V_{il_{ON/OFF}}$, input logic LO level		-0.2		0.8	V

(1) Buffered internal node, for information only.

SUPPLY MONITOR PARAMETERS

Test conditions $V_{DD} = 4.0V$ to $8.0V$, MODE pin = 1 unless otherwise stated



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PARAMETER	UNDERVOLTAGE			OVERVOLTAGE			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
TOL ₊₁₂ , Monitor tolerance.	-6 (11.28)	-8 (11.04)	-10 (10.8)	+10 (13.2)	+15 (13.8)	+20 (14.4)	% (V)
TOL ₊₅ , Monitor tolerance.	-6 (4.74)	-8 (4.62)	-10 (4.5)	+10 (5.5)	+15 (5.75)	+20 (6.0)	% (V)
TOL _{+2.175} , Monitor tolerance.	-6 (2.04)	-8 (2.00)	-10 (1.96)	+10 (2.39)	+15 (2.5)	+20 (2.81)	% (V)
TOL ₋₅ , Monitor tolerance.	-10 (-4.5)	-12.5 (-4.375)	-15 (-4.25)	+15 (-5.75)	+20 (-6.0)	+25 (-6.25)	% (V)
TOL ₋₁₂ , Monitor tolerance.	-10 (-10.8)	-12.5 (-10.50)	-15 (-10.20)	+15 (-13.8)	+20 (-14.4)	+25 (-15)	% (V)

TIMING SPECIFICATION

Test conditions $V_{DD} = 4.0V$ to $8.0V$ unless otherwise stated, see timing diagrams for definitions

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
T _{SU} , Delay from ON/OFF to POWER OUT going active.	ON/OFF transition from Hi to Lo	64		128	ms
T _{SD} , Delay from ON/OFF to POWER GOOD	ON/OFF transition from Lo to HI	32		64	ms
T _{PGD} , Delay from POWER OUT to POWER GOOD going active	V _{DD} = 4.0v	350	370		ms
T _{HU} , Delay from POWER GOOD going inactive to POWER OUT going inactive	After ON/OFF Lo to HI transition.		2		ms
T _{BL} , Blanking period for monitored inputs during start up.	Signals from all active monitor inputs blanked during this period.	115	116		ms
T _{RTO} , Restart time-out after an undervoltage shutdown	V _{DD} = 4.0V.	1.0	3.5		s
T _{DB} , Debounce period for SD input	V _{DD} = 5.0V	80		110	μs
T _{DBM} , Debounce period for 5 monitor inputs.		80		110	μs
T _{EW} , Debounce period for EW input		80		110	μs

Rev A

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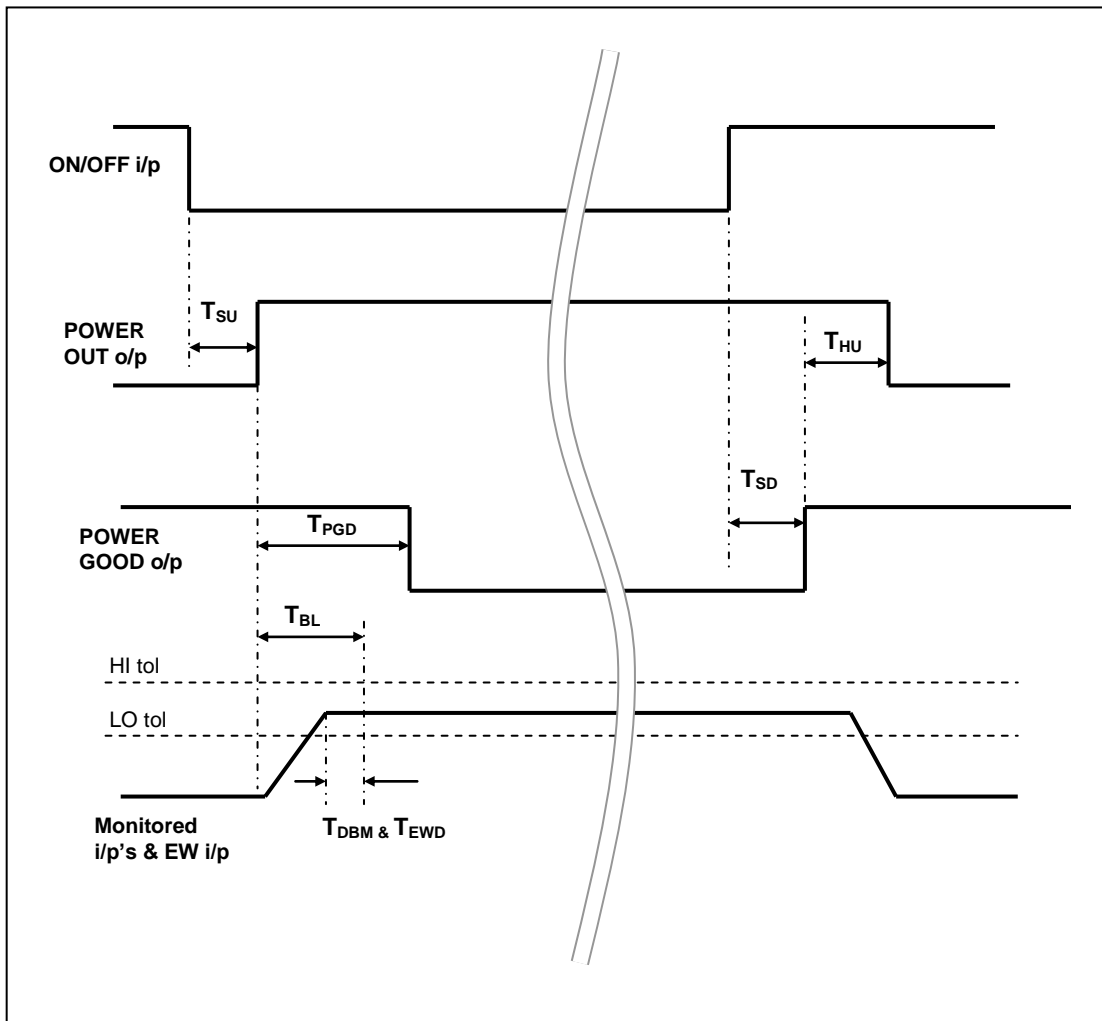
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T_{EW} , Sample period for EW input	EW input > threshold for $>T_{EW}$ during T_{RTO}	32			ms
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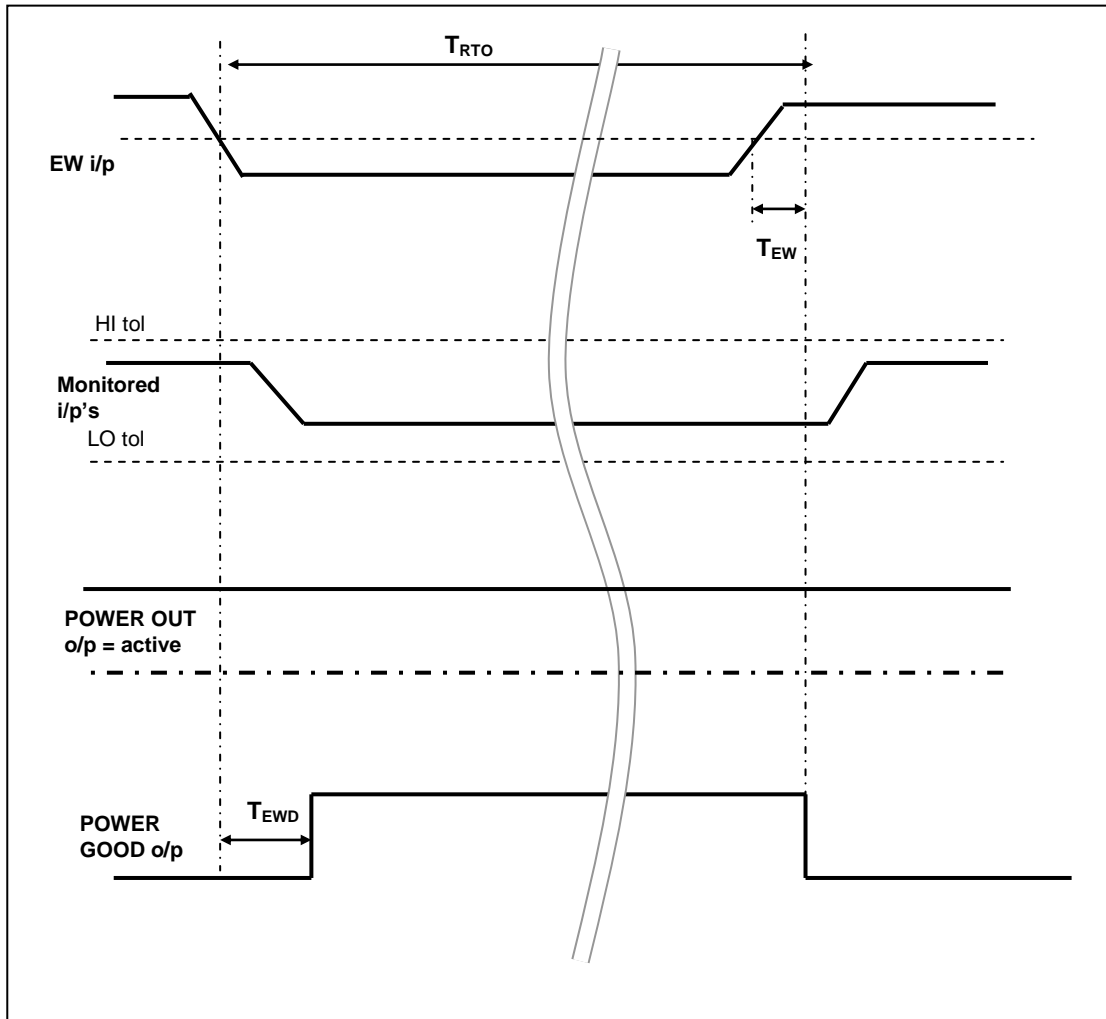
TIMING/DEFINITION DIAGRAM, MODE = Hi, SD < threshold.

Normal start up and shutdown.



TIMING/DEFINITION DIAGRAM, MODE = Hi, SD< threshold.

Response to EW input





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Power Good ASIC

GENERAL DESCRIPTION

The POWER GOOD CHIP (PGC) is designed to perform all of the housekeeping and warning functions normally required on a quality switch-mode power supply, (SMPS).

The power supply status is indicated on 2 digital outputs, POWER GOOD and POWER OUT. These outputs are configured as open drain mosfets for flexible interfacing to other circuitry within the SMPS. Typically the POWER OUT output is used to directly control the SMPS and the POWER GOOD output is used as a status flag for other sections of the system.

Power supply monitoring is accomplished by continuously sensing conditions on either 6 or 8 analogue inputs. The number of inputs active is selected by the MODE input. In addition to the supply voltage monitoring inputs, +12, +5, -5 and -12, there are 4 others, +2.175, SD, EW and ON/OFF which have special functions.

Their detailed action is discussed in later sections but in most applications the ON/OFF input senses the contacts of the power switch on the equipment which when closed, causes the POWER OUT output to become active and this in turn is used to turn on the SMPS.

The SD and +2.175 inputs receive signals from operating blocks within the pc system and EW monitors the switching waveform on the isolated output side of the SMPS and therefore provides an early warning of impending power failure.

The PGC differentiates between failure modes based on the state of the EW input prior to, or during, the event.

Normally the off condition caused by a failure requires that the ON/OFF input is cycled Hi then Lo to restart the SMPS, i.e. the result of a failure is latched on POWER OUT and POWER GOOD outputs

If, however the failure occurred when the EW input was below it's threshold the PGC will attempt to restart after 1 second provided that the ON/OFF input is held Lo.

All monitoring inputs are debounced to ensure transients do not cause malfunctions in the control system.

DESCRIPTION OF FUNCTION

ON/OFF input.

This is normally controlled from a low voltage switch on the equipment and is active when Lo. When the ON/OFF input is in the off state, i.e. Hi, both the POWER OUT and POWER GOOD outputs are in the inactive state.

When the ON/OFF input is taken to the on condition, the POWER OUT output will become active after a specified delay. The POWER GOOD output will become active a pre defined delay after POWER OUT became active provided that all the supplies monitored settle within their respective tolerances before the end of the delay period.

The above reflects a successful start up sequence. Faults detected by the SD or EW inputs can modify the status of POWER OUT and POWER GOOD as discussed later in the description.

When the state of the ON/ OFF input is changed from on to off, Lo to Hi, the POWER GOOD output goes to its inactive state. The POWER OUT output will remain active for a predetermined delay after the POWER GOOD output went inactive before switching to the inactive state.

The ON/OFF input has an internal pull up current source to the VDD pin on the package so the input may be left floating if required.



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VREF

The PGC has a precision 2.5 volt reference on chip which is trimmed during production to better than +/- 1.25%. All thresholds associated with the 5 monitor, SD and EW inputs use this reference or voltages derived from it.

Monitor inputs +12, +5, +2.175, -5 and -12

Four of the five inputs, +12, +5, -5 and -12, have resistive voltage dividers associated with them. The reference for the networks on the +12 and +5 inputs is GND and VREF for the -5 and -12. Details of the under and over voltage trip levels can be obtained from the electrical parameter table.

There is no resistor network associated with the +2.175 input which, therefore, has a very high input impedance. Threshold voltages can be adjusted by adding an appropriate resistor divider network to any of the monitor inputs although care should be taken to minimise errors caused by input impedance.

UNDER VOLTAGE DETECTION

An undervoltage condition can occur on the output of a SMPS as the result of three main conditions, these are:

- A fault on the power input side of the SMPS.
- A fault on the output side of the SMPS.
- A transient condition at the SMPS starts up.

The internal circuitry within the PGC is designed to differentiate between these conditions and give an appropriate response.

A fault on the input side of the SMPS would typically cause the output voltages being monitored to drop below their undervoltage thresholds at a later time. The EW signals defines that the undervoltage condition is being caused by EW being below tolerance and not an output fault.

The EW input is active when the voltage is less than its threshold of 2.5V. It has a fairly complex logic function to prevent false shutdown. This involves negative peak detection, debounce counting, ripple rejection, and a restart function for the POWER GOOD output. The signal at the EW input is likely to have a ripple waveform corresponding to the AC input of the power supply, which would normally be based on 50 or 60Hz. The POWER GOOD output will go inactive when the voltage on EW is lower than 2.5V for longer than its debounce period.

The EW input becoming active also starts a 1s time out for the detection of an undervoltage condition on the monitor inputs, or a shutdown command produced when SD is taken above its threshold. If at the end of this time there has been no corresponding undervoltage or shutdown, then the EW input will be re-examined. If the voltage level on EW is still below its threshold, the POWER OUT output will go inactive and the supply will be latched off.

If however, the level on the EW input has been above its threshold for the previous 32ms, then the POWER GOOD output will become active again.



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The PGC reacts to an output fault in the following way. When the PGC and SMPS are operating normally with the ON/OFF input is in the ON state, Lo, the PGC will monitor all of the input voltages selected. If any voltage falls below its under voltage threshold then the POWER GOOD and POWER OUT outputs will immediately go to an inactive state, turning off the SMPS.

To restart the system, the ON/OFF input must be cycled from the Lo to Hi to Lo condition since the off condition after this fault is latched.

When the SMPS is starting up it takes time for the voltages being monitored to settle within tolerance. So during start up, all indications from the under voltage detection circuitry are inhibited for a fixed delay to allow the monitored supplies to settle within tolerance. If after that period the monitored voltages are still undervoltage, POWER OUT will go inactive and the system will need to be restarted as outlined as above.

OVER VOLTAGE DETECTION

When the PGC and SMPS are operating normally with the ON/OFF input in the ON Lo, state. The PGC will monitor all of the input voltages selected. If any voltage rises above its over voltage threshold for a period greater than its debounce period both the POWER OUT and POWER GOOD outputs will immediately go to the inactive state. The system can only be restarted as outlined above.

SD INPUT (and optional second input, SD1)

When the PGC and SMPS are operating normally with the ON/OFF input in the on Lo, state. If then the SD input voltage exceeds its threshold for greater than its debounce period, the POWER OUT and POWER GOOD outputs immediately go to the inactive state.

This action is independent of the status all other monitored inputs.

The POWER OUT output will remain inactive until the ON/OFF input is cycled from Lo to Hi to Lo to initiate another start up sequence.

The inputs have pull up current sources referenced to the VDD pin on the package.

The SD input could be used with other circuitry to sense an over current condition in some applications.

MODE

The PGC has two modes of operation, which are selected by the state on the MODE pin and are as follows.

Disable Negative monitor inputs (MODE Pin Lo) This model allows the PGC to be used with power supplies which do not have negative outputs whilst still performing the full functions on all of the positive inputs.

Enable Negative monitor Inputs (MODE Pin Hi). This mode will allow full function on all input voltages.

The input has an internal current source connected to the VDD pin. The input may be left open for the logic Hi condition.



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INTERNAL OSCILLATOR

The PGC has an internal oscillator that provides a timebase for the control logic. The oscillator is trimmed during production to a typical frequency of 32kHz. Over the full operating temperature the oscillator frequency will remain within the range $\pm 25\%$ of this value.

The buffered clock signal is available as a bond option for an additional output but is not available on the 14 pin package version shown in this specification.

All time parameters in this specification are derived as a clock count based on the internal oscillator and will be subject to the same tolerances as the oscillator.